CLAIMS

1. An elevator control apparatus comprising:

a first processing portion and a second processing portion that perform calculations regarding control of an elevator according to a duplexed system;

a first clock that transmits a first clock signal to the first processing portion;

a second clock that transmits a second clock signal to the second processing portion; and

a clock abnormality detecting circuit that detects abnormalities in the first clock signal and the second clock signal, the first clock signal and the second clock signal being input to the clock abnormality detecting circuit,

wherein the clock abnormality detecting circuit counts numbers of pulses of the first clock signal and the second clock signal, and detects abnormalities in the first clock signal and the second clock signal based on a difference between the numbers of the pulses.

2. An elevator control apparatus according to Claim 1, wherein the clock abnormality detecting circuit comprises a monitored counter that counts a number of pulses of one of the first clock signal and the second clock signal, and a monitoring counter that counts a number of pulses of the other of the first clock signal

and the second clock signal,

a preset data value that is a count value at a time of starting counting by the monitored counter is set larger than a preset data value that is a count value at a time of starting counting by the monitoring counter,

a count number of the monitored counter is reset when the monitoring counter carries over, and

abnormalities in the first clock signal and the second clock signal are detected through carry-over of the monitored counter.

3. An elevator control apparatus according to Claim 2, wherein the monitoring counter comprises a first monitoring counter that counts a number of pulses of the first clock signal, and a second monitoring counter that counts a number of pulses of the second clock signal, and

the monitored counter comprises a first monitored counter that counts a number of pulses of the first clock signal, and a second monitored counter that counts a number of pulses of the second clock signal.

4. An elevator control apparatus according to Claim 2, wherein the preset data value of the monitoring counter can be arbitrarily set.

5. An elevator control apparatus according to Claim 2, wherein integrity of the clock abnormality detecting circuit can be confirmed by deliberately making a clock signal, which is input to the monitored counter, abnormal in a test mode.

6. An elevator control apparatus according to Claim 5, wherein the clock abnormality detecting circuit comprises a multiplying circuit that multiplies a clock signal input to the monitored counter in the test mode.